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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/689,265	10/20/2003	Brian L. Smith	5681-11500	2888

35690 7590 02/06/2006

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EXAMINER	
RADOSEVICH, STEVEN D	
ART UNIT	**PAPER NUMBER**
2138	

DATE MAILED: 02/06/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/689,265	SMITH, BRIAN L.	
	Examiner	Art Unit	
	Steven D. Radosevich	2138	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☐ Claim(s) _____ is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☒ Claim(s) *6* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 October 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claims 1-20 are present for examination.

Priority

Acknowledgement is made that no priority either foreign or domestic is claimed for this application and as such the filing date (10/20/2003) is being used for this examination.

Information Disclosure Statement

Acknowledgement is made that no Information Disclosure Statement (IDS) was provided with the application.

Drawings

The drawings (3A-C and 4) are objected to since it is unclear to the examiner how in these figures a numerical two "2" is represented in a bit patter; only ones "1" and zeros "0" are present in a binary bit patterns. Appropriate correction is required.

Claim Objections

Claim 6 is objected to because of the following informalities: it is unclear to the examiner if the "turnaround" in line 2 of the claim is intended to be the same as the "turn-around" described in the specification. Appropriate correction is required and for the purposes of this examination the "turnaround" in line 2 of the claim will be treated as being the same as the "turn-around" described in the specification.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claim 12 recites the limitation "claim 4" in line 1 of the claim. There is insufficient antecedent basis for this limitation in the claim. For the purposes of this examination examiner will treat claim 12 as depending on claim 7.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-20 are rejected under 35 U.S.C. 102(b) as being anticipated by Firth et al. (US 2002/0138802 A1).

As per claim 1, Firth teaches a method for testing comprising:

Storing a first value (identifier – 0093 lines 3-4);

Storing a second value (identifier – 0093 lines 3-4);

Receiving a clock signal (clocking – 0093 line 7);

Selecting either said first value or said second value for inclusion in a test pattern in response to said clock signal (0093 – lines 4-6);

Wherein determining whether to select either said first value or said second value on a given clock cycle is determined according to a predetermined test pattern sequence (applying two or more Marinescu tests - 0092 lines 4-6).

As per claim 2, Firth teaches the method described above as per claim 1, wherein said test pattern sequence comprises a plurality of indications (identifier – 0093 lines 3-4) indicating either said first value or said second value.

As per claim 3, Firth teaches the method described above as per claim 2, wherein said first value is stored in a first register location, and said second value is stored in a second register location, and wherein both said first and second register locations correspond to a same link signal line (Examiner believes it to be inherent – 0093 lines 1-10).

As per claim 4, Firth teaches the method described above as per claim 3, further comprising driving values of said test pattern from a first component to a second component (see figures 2, 3, and 4).

As per claim 5, Firth teaches the method described above as per claim 4, wherein each of said first component and said second component alternate driving values of said test pattern during a sixteen test cycle sequence (see figure 2, 306 and 303 - figure 3, X - 0004 lines 3-5, and 0093 line 2).

As per claim 6, Firth teaches the method described above as per claim 5, wherein said alternate driving of values by said first component and said second component is separated by one or more turnaround cycles (0089 lines 1-8, figure 3).

As per claim 7, Firth teaches a system comprising:

A first component (301 – figure 3);

A second component (305 – figure 3);

A link coupling said first component to said second component (see figure 3);

Wherein said first component is configured to:

Determine whether to select either a first stored value or a second stored value (memory test – 0091 line 8 and 0092 lines 4-6) for inclusion in a test pattern (output – 0087 lines 9-10 and see figure 3) on a given clock cycle, wherein said determination is based upon a predetermined test pattern sequence (0091 – lines 6-9, 301 – figure 3, and 0093 lines 4-10).

As per claim 8, Firth teaches the system as per claim 7, wherein said predetermined test pattern sequence comprises a sequence of sixteen indications (0004), each of said indications indicating either said first or said second value (Examiner believes it to be inherent – 0093 lines 1-10).

As per claim 9, Firth teaches the system described above as per claim 8, wherein the link comprises a signal line, and wherein said first value is stored in a first register location, and said second value is stored in a second register location, and wherein both said first and second register locations correspond to a same link signal line (Examiner believes it to be inherent – 0093 lines 1-10).

As per claim 10, Firth teaches the system as described above as per claim 9, wherein said first component is configured to drive values of said test pattern to said second component (see figure 3 and control data - 0091 lines 6-9).

As per claim 11, Firth teaches the system as described above as per claim 10, wherein each of said first component and said second component alternate driving values of said test pattern during a sixteen indication test cycle sequence (see figure 2, 306 and 303 - figure 3, X - 0004 lines 3-5, and 0093 line 2)

As per claim 12, Firth teaches the system as described above in claim 7, wherein each of said first component and said second component alternate driving values of said pattern during a sixteen test cycle sequence (0004), wherein each of said components drives two consecutive values in turn (Examiner believes it to be inherent – 0093 lines 1-10 and 0004)

As per claim 13, Firth teaches a component comprising:

A plurality of drivers (BIST dictionary – figure 4) each of said drivers coupled to a separate signal line of a plurality of signal lines of a link (see figures 3 and 4);

A register (403 - figure 4) configured to store a first bit pattern and a second bit pattern (tests – 0092 lines 4-6), wherein each bit of said first bit pattern and said second bit patter corresponds to a signal line of said link (Examiner believes it to be inherent – 0093 lines 1-10);

A test pattern sequence unit, wherein said unit is configured to indicate a predetermined sequence in which values are to be selected from either said first bit pattern or said second bit patter (402 – figure 4 and 0102 lines 4-5); and

Control circuitry configured to generate a test pattern (401 – figure 4 and 0102 lines 1-3), wherein on a given test cycle said circuitry is configured to select a value from either said first bit pattern or said second bit patter in response to detecting an indication in said test pattern sequence which indicates one of said first bit patter and said second bit pattern is to be accessed (301 - figures 3, 4, and 0093 lines 1-10).

As per claim 14, Firth teaches the component as recited in claim 13, wherein said predetermined test pattern sequence comprises a plurality of indications (X – 0004 – 0010), each of said indications indicating either said first value or said second value (identifier for each test – 0093 lines 1-4).

As per claim 15, Firth teaches the component as recited in claim 14, wherein each test cycle said control circuitry iterates through said test patter sequence in order to ascertain a bit pattern indication for each test cycle (figures 3, 4, and 0091 lines 6-9).

As per claim 16, Firth teaches the component as recited in claim 15, wherein said component is configured to drive values of said test pattern via said link (see figures 3 and 4).

As per claim 17, Firth teaches the component as recited in claim 16, wherein during a sixteen test cycle sequence (X – 0004 – 0010, and 0093 line 2), said component is configured to alternate between driving two sequential values (read/write – 0097 line 1-5 and 0099) of said test pattern and receiving two values of said test pattern (read/write – 0097 line 1-5 and 0099).

As per claim 18, Firth teaches to component as recited in claim 13, further comprising a plurality of receivers coupled to said link (300 – figure 3, rows and columns – 0102 line 5), and wherein said component includes pattern checking circuitry configured to compare values received via said link to expected values (003 lines 9-11 and 0094 lines 5-7).

As per claim 19, Firth teaches to component as recited in claim 13, wherein said register comprises N bits, said first pattern comprises N/2 bits, said second pattern

comprises N/2 bits, and said link comprises N/2 signal lines, and wherein each signal line corresponds to one bit of each of said first pattern and said second patter (Examiner believes it to be inherent – 0093 lines 1-10).

As per claim 20, Firth teaches to component as recited in claim 19, wherein each signal line is coupled to receive a value from a multiplexer (403 – figure 4), wherein each multiplexer is coupled to one bit of said first pattern and one bit of said second pattern (tests – 0091 lines 6-9), and wherein said control circuitry is configured to control each multiplexer to convey from each multiplexer a bit from either said first pattern or said second pattern (Examiner believes it to be inherent – 0093 lines 1-10).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Steven D. Radosevich whose telephone number is 571-272-2745. The examiner can normally be reached on 9am-5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on 571-272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applicátions may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Steven D. Radosevich
Examiner
Art Unit 2138

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